WHAT IS CLAIMED IS:

1. A synchronous DRAM comprising:

a first input terminal which receives an external clock signal;

a second input terminal which receives a clock enable signal;

a plurality of third input terminals which receive command signals;

a fourth input terminal which receives an external power supply voltage; and

a voltage limiter circuit which generates an internal power supply voltage lower than said external power supply voltage; and

a control circuit which receives said command signals in synchronism with said external clock signal,

wherein said DRAM is in a power down mode when said clock enable signal is low,

wherein said DRAM is out of said power down mode when said clock enable signal is high,

wherein said voltage limiter circuit is not in operation when said DRAM is in said power down mode, and

wherein said voltage limiter circuit is in operation when said DRAM is out of said power down mode.

2. A synchronous DRAM according to claim 1,

wherein said voltage limiter circuit stops operating in synchronism with receiving a set of command signals.

3. A synchronous DRAM according to claim 1,

wherein said voltage limiter circuit starts operating in synchronism with a rising edge of said clock enable signal.

4. A synchronous DRAM comprising:

a first power supply circuit which receives an externally supplied voltage and outputs an internal supply voltage; and

a second power supply circuit which receives said externally supplied voltage and outputs said internal supply voltage,

wherein said first power supply circuit is not in operation when a semiconductor device is in a power down mode for said synchronous DRAM, and

wherein said second power supply circuit is continuously in operation during said power down mode.

5. A synchronous DRAM comprising:

a first power supply circuit which receives an externally supplied voltage and outputs an internal supply voltage; and

a second power supply circuit which receives said externally supplied voltage and outputs said internal supply voltage,

wherein said synchronous DRAM operates in a power down mode and a mode, prior to said power down mode, in which said synchronous DRAM receives a clock signal and stands by for a power down mode command signal to begin said power down mode,

wherein said first power supply circuit is not in operation when said semiconductor device is in said power down mode, and

wherein said second power supply circuit is continuously in operation during said power down mode.